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ABSTRACT OF THE DISCLOSURE

A design verification system that verifies the operation of multi-processor architecture by generating test programs. in which the behavior of the processor, when executing the test program, is evaluated against the behavior required by the design specification. The test program generator produces scenarios for a multi-processor design in which non-unique results may occur. The system is provided with facilities to report expected outcomes, and to evaluate the validity of non-unique results in multiple resources under conditions of non-unique result propagation and dependencies among adjacent and non-adjacent resources.